IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Faust**	§	Group Art Unit: **2829**
	§	
Serial No.: **10/821,044**	§	Examiner: **Nguyen, Vinh**
	§	
Filed: **April 8, 2004**	§	Attorney Docket No.: **AUS920040056US1**
	§	
For: **Apparatus, Method, and Computer Program Product for Monitoring and Controlling a Microcomputer Using a Single Existing Pin**	§	

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

35525
PATENT TRADEMARK OFFICE
CUSTOMER NUMBER

RESPONSE TO OFFICE ACTION

Sir:

No fees are believed to be required. If, however, any fees are required, I authorize the Commissioner to charge these fees which may be required to IBM Corporation Deposit Account No. 09-0447. No extension of time is believed to be necessary. If, however, an extension of time is required, the extension is requested, and I authorize the Commissioner to charge any fees for this extension to IBM Corporation Deposit Account No. 09-0447.

In response to the Office Action of June 7, 2006, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original): A method for monitoring and controlling a device using only one input/output (I/O) communication pin of said device, said method comprising:

configuring said I/O pin to be used to transmit and receive data;

generating logical ones using pulses that are a first length and generating logical zeros pulses that are a second length; and

communicating with said device utilizing said generated logical ones and generated logical zeros by transmitting said logical ones and zeros to said device utilizing said I/O pin.

2. (Original): The method according to claim 1, further comprising the steps of:

configuring said I/O pin by connecting said I/O pin to a first node of a pull-up resistor and connecting a second node of said pull-up resistor to a power source; and

said I/O pin being configured as an open collector output that will serve as both an input pin and an output pin.

3. (Original): The method according to claim 1, further comprising the steps of:

generating said logical ones and logical zeros using an external device that is coupled to said device using said I/O pin.

4. (Original): The method according to claim 3, further comprising the steps of:

connecting a first node of a second resistor included within said external device to a power source;

connecting a second node of said second resistor to a first node of an LED;

connecting a second node of said LED to a first communication pin of said external device;

connecting said second node of said LED to a first node of a switch; and

connecting a second node of said switch to ground.

5. (Original): The method according to claim 4, further comprising the steps of:

connecting said first communication pin of said external device to said I/O pin of said device; and

generating said logical ones and logical zeros by opening and closing said switch.

6. (Original): The method according to claim 5, further comprising the steps of:

generating a bit stream by repeatedly opening and closing said switch to generate said logical ones and said logical zeros;

generating said logical ones by closing said switch for a first length of time; and

generating said logical zeros by closing said switch for a second length of time.

7. (Original): The method according to claim 5, further comprising the steps of:

connecting said first communication pin of said external device to said I/O pin of said device; and

receiving, by said first communication pin of said external device, data transmitted by device utilizing said I/O communication pin; and

outputting said data using said LED.

8. (Original): The method according to claim 3, further comprising the steps of:

connecting a first node of a bi-directional driver that is included in said external device to a first communication pin of said external device; and

connecting said first communication pin to said I/O pin of said device.

9. (Original): The method according to claim 8, further comprising:

generating said logical ones and said logical zeros by said external device and outputting said logical ones and said logical zeros using said first communication pin.

10. (Original): A system for monitoring and controlling a device using only one input/output (I/O) communication pin of said device, said system comprising:

said I/O pin being configured to both transmit and receive data;

said I/O pin for receiving and transmitting logical ones that are pulses that are a first length and logical zeros that are pulses that are a second length; and

said I/O pin for communicating with said device utilizing said generated logical ones and generated logical zeros by transmitting said logical ones and zeros to said device utilizing said I/O pin.

11. (Original): The system according to claim 10, further comprising:

said I/O pin being configured by connecting said I/O pin to a first node of a pull-up resistor and connecting a second node of said pull-up resistor to a power source; and

said I/O pin being configured as an open collector output that will serve as both an input pin and an output pin.

12. (Original): The system according to claim 10, further comprising:

said logical ones and logical zeros being generated using an external device that is coupled to said device using said I/O pin.

13. (Original): The system according to claim 12, further comprising:

a first node of a second resistor included within said external device connected to a power source;

a second node of said second resistor connected to a first node of an LED;

a second node of said LED connected to a first communication pin of said external device;

said second node of said LED connected to a first node of a switch; and

a second node of said switch connected to ground.

14. (Original): The system according to claim 13, further comprising:

said first communication pin of said external device connected to said I/O pin of said device; and

said logical ones and logical zeros being generated by opening and closing said switch.

15. (Original): The system according to claim 14, further comprising:

a bit stream generated by repeatedly opening and closing said switch to generate said logical ones and said logical zeros;

said logical ones generated by closing said switch for a first length of time; and

said logical zeros generated by closing said switch for a second length of time.

16. (Original): The system according to claim 14, further comprising:

said first communication pin of said external device connected to said I/O pin of said device; and

said first communication pin of said external device for receiving data transmitted by device utilizing said I/O communication pin; and

said LED for outputting said data.

17. (Original): The system according to claim 12, further comprising:

a first node of a bi-directional driver that is included in said external device connected to a first communication pin of said external device; and

said first communication pin connected to said I/O pin of said device.

18. (Original): The system according to claim 17, further:

said logical ones and said logical zeros generated by said external device and outputting said logical ones and said logical zeros using said first communication pin.

19. (Original): A computer program product for monitoring and controlling a device using only one input/output (I/O) communication pin of said device, said product comprising:

instructions for configuring said I/O pin to be used to transmit and receive data;

instructions for generating logical ones using pulses that are a first length and generating logical zeros pulses that are a second length; and

instructions for communicating with said device utilizing said generated logical ones and generated logical zeros by transmitting said logical ones and zeros to said device utilizing said I/O pin.

20. (Original): The product according to claim 19, further comprising:

instructions for generating a bit stream by repeatedly opening and closing a switch that is external to said device and connected to said I/O pin to generate said logical ones and said logical zeros;

instructions for generating said logical ones by closing said switch for a first length of time; and

instructions for generating said logical zeros by closing said switch for a second length of time.

REMARKS/ARGUMENTS

Claims 1-20 are pending in the present application. Reconsideration of the claims is respectfully requested.

I. Interview

Applicant thanks Examiner Vinh Nguyen for his time during the telephone conference that was held on August 30, 2006. Applicant's claims were discussed. No agreement was reached. Applicant also thanks the Examiner for his offer to make the next office action a non-final action in the event that the Examiner does not find the arguments made herein to be persuasive.

II. 35 U.S.C. § 103, Obviousness

Claims 1-3, 8-13, and 17-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Application Publication 2004/0187049 issued to *West* in view of U.S. Patent 6,294,949 issued to *Kojima et al.* This rejection is respectfully traversed.

While the office action states that claim 13 is rejected, no art was applied against claim 13. Therefore, Applicant believes the inclusion of claim 13 in the rejection was a typographical error.

Applicant's independent claims describe similar features. Claim 1 is representative of the independent claims. Claim 1 recites generating logical ones using pulses that are a first length and generating logical zero pulses that are a second length; and communicating with said device utilizing said generated logical ones and generated logical zeros by transmitting said logical ones and zeros to said device utilizing said I/O pin.

West teaches, in paragraph 0045, comparing two voltage levels to determine whether a logic state of zero or a logic state of one will be output. Figure 3b teaches particular voltage levels and the resulting outputs for those voltage levels. Neither paragraph 0045 nor Figure 3b, however, teaches the length of pulses. Neither Figure 3b nor paragraph 0045 teaches logical ones that are a first length and logical zeros that are a second length.

More particularly, paragraph 0045 teaches that output ra has a logic state of one if Vra is greater than Vofa and a logic state of zero if Vra is not greater than Vofa. The output rb has a logic state of one if Vrb is greater than Vofb and a logic state of zero if Vrb is not greater than Vofb. Figure 3b provides example values for Vra, Vrb, Vofa, and Vofb and the resulting ra and rb outputs.

Applicant teaches logical one pulses that are a first length and logical zero pulses that are a second length. *West* does not provide any teaching at all as to pulse length. *West* teaches using voltage levels to determine whether a logical one or logical zero will be output. *West*, however, does not teach

what the logical one and logical zero pulses will look like. *West* provides no teaching regarding the parameters of logical one and logical zero pulses.

The office action acknowledges that *West* does not teach generating logical ones using pulses that are a first length and generating logical zero pulses that are a second length; and communicating with said device utilizing said generated logical ones and generated logical zeros by transmitting said logical ones and zeros to said device utilizing said I/O pin. The office action asserts that *Kojima* teaches generating logical ones using pulses that are a first length and generating logical zero pulses that are a second length in column 7, lines 14-24, of *Kojima*.

> The voltage drive circuit 100 includes a pulse generator P1 generating the input signal A as a differential signal. The input signal A can take two values including a high value whose logic value is one, and a low value whose logic value is zero. When the input signal A is high, it means that the input signal A takes the high value, a positive output P1p from the pulse generator P1 becomes high and a negative output P1m becomes low. When, on the other hand, the input signal A is low, it means that the input signal A takes the low value, the positive output P1p from the pulse generator P1 becomes low and the negative output P1m becomes high.

Kojima, column 7, lines14-24.

The cited section of *Kojima* teaches a signal that is a pulse that has a high value and a low value. Such a pulse is depicted in Figure 2. These values are different values of the amplitude of a pulse. An amplitude is a height, not a length. An amplitude is a displacement in a y direction, while a length is a displacement in an x direction. The high and low values of *Kojima* are not length values. In contradistinction to the teachings of *Kojima*, Applicant claims pulses that are differing lengths.

The office action asserts that *Kojima* teaches communicating with said device utilizing said generated logical ones and generated logical zeros by transmitting said logical ones and zeros to said device utilizing said I/O pin; however, the Examiner does not refer to any section of *Kojima* that supposedly teaches this feature.

The combination of *West* and *Kojima* does not teach or suggest Applicant's claims because the combination does not teach generating logical ones using pulses that are a first length and generating logical zero pulses that are a second length; and communicating with said device utilizing said generated logical ones and generated logical zeros by transmitting said logical ones and zeros to said device utilizing said I/O pin. Therefore, the combination of *West* and *Kojima* does not render Applicant's claims obvious.

III. Objection to Claims

The Examiner has stated that claims 4-7 and 14-16 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The Office Action states:

> The prior arts of record are fail to disclose the combination of the based claim with the method according to claim 3, further comprising the steps of:
> connecting a first node of a second resistor included within said external device to a power source;
> connecting a second node of said second resistor to a first node of an LED;
> connecting a second node of said LED to a first communication pin of said external device;
> connecting said second node of said LED to a first node of a switch; and
> connecting a second node of said switch to ground.

Office Action, dated June 7, 2006, pages 4-5.

It appears that there are several typographical errors in the office action regarding which claims are objected to but would be allowable if rewritten. Based on the statement reproduced above, Applicant understands the features of "connecting a first node of a second resistor included within said external device to a power source; connecting a second node of said second resistor to a first node of an LED; connecting a second node of said LED to a first communication pin of said external device; connecting said second node of said LED to a first node of a switch; and connecting a second node of said switch to ground" to be patentable. These features appear in claims 4 and 13. Furthermore, no art was cited against claims 4-7 or 13-16 in paragraph 2, on pages 2-4. Therefore, Applicant believes the Examiner meant to object to claims 4-7 and 13-16, and to state that claims 4-7 and 13-16 would be allowable if rewritten in independent form.

IV. Conclusion

It is respectfully urged that the subject application is patentable over the cited prior art and is now in condition for allowance.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: September 7, 2006

Respectfully submitted,

/Lisa L.B. Yociss/

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